Use the formulae for power consumption $P$ and delay $\tau$ of a CMOS circuit from the lecture notes. The threshold voltage $V_t$ can be considered to be negligible compared to the voltage $V_{dd}$.

**Task 1: Dynamic Voltage Scaling and Dynamic Power Management (Non-Negligible Threshold Voltage)**

Suppose that the power consumption $P(f)$ of a given CMOS processor at frequency $f$ is:

$$P(f) = \left(10 \left(\frac{f}{100\text{MHz}}\right)^3 + 20\right) \text{mWatt}$$

To reduce the power consumption, one can adjust the execution frequency by applying the dynamic voltage scaling technique. The maximum (resp. minimum) available frequency $f_{\text{max}}$ (resp. $f_{\text{min}}$) is 1000MHz (resp. 50MHz). Frequency switching has negligible overhead and the processor can operate at any frequency between 50MHz and 1000MHz. One can also apply the dynamic power management to turn the processor to the sleep mode (or turn the processor off) to reduce the power consumption. When the processor is in the sleep mode, it consumes no power. However, turning the processor on to the run mode requires additional energy consumption, i.e., $3 \times 10^{-5}$ Joule (switching from run mode to sleep mode consumes no energy). Turning on/off the processor can be done instantly.

The system has three jobs to execute:

<table>
<thead>
<tr>
<th></th>
<th>arrival time</th>
<th>deadline</th>
<th>execution cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau_1$</td>
<td>0</td>
<td>2 ms</td>
<td>100000</td>
</tr>
<tr>
<td>$\tau_2$</td>
<td>2ms</td>
<td>6 ms</td>
<td>100000</td>
</tr>
<tr>
<td>$\tau_3$</td>
<td>6ms</td>
<td>7 ms</td>
<td>80000</td>
</tr>
</tbody>
</table>

The processor is in the run mode at time 0 and is required to be in the run mode at time 7 ms.

1. The energy consumption to execute $C$ cycles is $\frac{C \cdot P(f)}{f}$. There is a critical frequency $f_{\text{crit}}$ between 50MHz and 1000MHz at which the energy consumption to execute any $C$ cycles is minimized. What is the critical frequency $f_{\text{crit}}$ of the processor?

2. When the processor is idle at frequency $f_{\text{min}}$ for $t$ seconds, the energy consumption is $P(f_{\text{min}}) \times t$. The break-even time is defined as the minimum idle interval, for which it is worthwhile to turn the processor off. What is the break-even time of the processor?
3. A workload-conserving schedule is defined as a schedule which always executes some jobs when the ready queue is not empty. Please provide the workload conserving schedule for the three jobs which minimizes the energy consumption without violating the timing constraints. For this, consider the critical frequency \( f_{\text{crit}} \) as the frequency for active task execution. What is the energy consumption of the schedule?

4. Could you provide another workload-conserving schedule without violating the timing constraints for the three jobs with less energy consumption than the schedule in (c)? If yes, please write it down. If not, please prove the optimality of your derived schedule in (c).

5. Could you provide another schedule without violating the timing constraints for the three jobs that is not workload-conserving but with less energy consumption than the optimal workload-conserving schedule? If yes, please write the schedule down. If not, please show that optimality of workload-conserving schedules.

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**Task 2: Dynamic Voltage Scaling for Real-Time Tasks**

Let us consider a set \( J \) of aperiodic jobs as illustrated below. Suppose that the power consumption of the system is \( P(f) = (\frac{f}{10^6})^3 \) Watt and that the processor frequency can be any in the range \([10^5, 10^7]\) Hz.

<table>
<thead>
<tr>
<th>Job ID</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>arrival time (msec)</td>
<td>0</td>
<td>2</td>
<td>6</td>
<td>8</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>absolute deadline (msec)</td>
<td>8</td>
<td>12</td>
<td>10</td>
<td>20</td>
<td>25</td>
<td>15</td>
</tr>
<tr>
<td>cycles (( \times 10^3 ))</td>
<td>1</td>
<td>6</td>
<td>8</td>
<td>2</td>
<td>5</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 1: Job set \( J \)

1. What is the optimal schedule to minimize the energy consumption without deadline misses for job set \( J \)? What is the energy consumption of the resulting schedule? [hint: apply the YDS algorithm]

2. Suppose that we do not know a job before it arrives to the system. What is the resulting schedule by applying YDS algorithm on-line for job set \( J \)?

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**Task 3: Dynamic Power Management**

Consider a micro-controller of type TI-MLP230, which consumes \( P_{\text{active}} = 1.2 \) mW in the ACTIVE mode or \( P_{\text{sleep}} = 90.0 \) \( \mu \)W in the SLEEP mode. Several interrupts occur at times \( t = iT \), \( i \in \{0, 1, 2, \ldots\} \) to notify the processor about the arrival of new tasks. The processing of each task needs time \( t_{\text{task}} \). The transition from the SLEEP mode to the ACTIVE mode lasts \( t_2 \); the transition from the ACTIVE mode to the SLEEP mode lasts \( t_1 \) (see figure). We assume that the micro-controller remains idle during these transitions. Also, for simplicity, we assume that the power changes continuously and linearly during the transitions. For the energy supply of the system, an energy source (battery) with \( E_{\text{bat}} = 25.0 \) kJ is deployed.
1. Initially, neglect the transition times \( t_1 = t_2 = 0 \). Assume that after each interrupt, the processor gets into the ACTIVE mode and executes a task for \( t_{\text{task}} = 2 \text{ sec} \). After the execution of the task, the processor returns into the SLEEP mode. Which condition must period \( T \) satisfy so that the system can execute at least \( 5 \cdot 10^6 \) calculations (tasks)? How does this condition affect the maximum life time of the processor?

2. Next, assume that \( t_1 = 25 \text{ ms} \), \( t_2 = 75 \text{ ms} \), \( t_{\text{task}} = 100 \text{ ms} \), and \( T = t_1 + t_2 + t_{\text{task}} \). At time \( t = 0 \) the processor is in SLEEP mode. Please sketch the power consumption function \( P(t) \) of the processor in the given diagrams as follows:

- **Schedule S1**: Transition to the ACTIVE mode follows directly after an interrupt. After the task execution, i.e., after \( t_{\text{task}} \), the processor returns immediately to the SLEEP mode.

- **Schedule S2**: If the processor is in the SLEEP mode when an interrupt occurs, then transition to the ACTIVE mode happens immediately. After the task execution, the processor decides whether to return to the SLEEP mode or to remain in the ACTIVE mode in order to execute the next task without delay when the next interrupt occurs. The processor makes this decision aiming at minimizing the energy consumption.

3. Compute the energy difference \( \Delta E \), which can be saved on average per period \( T \) (200 ms) when Schedule S2 is used instead of Schedule S1.
4. Consider a Schedule S-OPT, for which the following condition must hold: the task denoted by the \( i \)–th interrupt must have finished by the time the \( (i + 1) \)–th interrupt occurs. S-OPT must serve the arriving tasks with the minimum possible energy under the above condition. Please show the function \( P(t) \) for Schedule S-OPT in the given diagram below. Also, compute the energy difference \( \Delta E' \), which can be saved on average per period \( T \) when Schedule S-OPT is used instead of Schedule S1.

![Graph showing Schedule S-OPT](image)

**Task 4: Energy Harvesting**

Consider a processor with negligible leakage power dissipation and dynamic power dissipation specified as \( P_{\text{dynamic}} = \left( \frac{f}{\text{MHz}} \right)^3 \text{mW} \), where \( f \) is the frequency in Hz. The processor is put into a zero power state whenever it is idle. The set of hard real-time tasks of Table 2 needs to be executed on the processor:

<table>
<thead>
<tr>
<th>Tasks</th>
<th>( T_1 )</th>
<th>( T_2 )</th>
<th>( T_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period (ms)</td>
<td>6</td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>Relative Deadline (ms)</td>
<td>6</td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>Cycles (x10^3)</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 2: Characteristics of the hard real-time tasks to be executed.

All tasks initially arrive at time zero. The system has a battery with initial energy \( C \) microjoule (\( \mu J \)) and it is replenished by a constant power source of \( A \) microjoule per millisecond (\( \mu J/\text{ms} \)).

1. Assume \( C = 6 \, \mu J \), \( A = 0.5 \, \frac{\mu J}{\text{ms}} \) and \( f = 1 \, \text{MHz} \). Apply EDF scheduling and draw in Figure 1 the battery energy during the time interval \([0 \, \text{ms}, 12 \, \text{ms}]\).

2. Assume the battery does not run out of charge. Prove or disprove the following statement:

   To have the maximum possible battery energy after each hyper-period (12 ms), all tasks should run at the same frequency.

   *(Hint: providing main arguments or formal proof are both accepted.)*
Figure 1: Battery energy diagram.