ETH zürich

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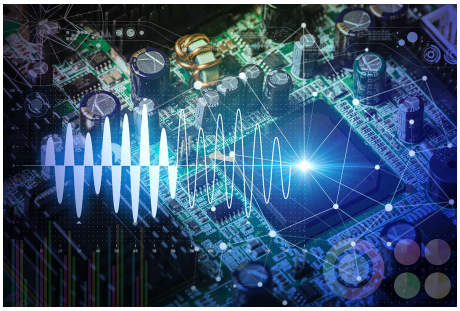
Advanced Functionality in Network Hardware

Master thesis proposal

The Internet has taken over the world. We consume and generate more traffic than ever, want our content to be available anywhere and at any time instantaneously. Consequently, networks have evolved to be complex systems with high reliability and performance requirements. At the same time, data privacy and protection become more pressing issues than ever.



While the Internet is where the innovation happens today, it is surprisingly hard to innovate the Internet itself. For the last couple of decades, the Internet architecture and infrastructure has become ossified with its limitations and obstacles. The core protocols of the Internet have remained the same, and the fixed functionality devices in the core of the Internet only exacerbated the problem. This is now changing with the advent of programmable networks.

Emerging programmability of networking devices opens up an entire set of possibilities to implement new functionality in the data plane. However, today's programmable network hardware is still very limited and resource-constrained. For example, the programmable switches one can buy "off the shelf"[1] do not support any cryptographic operations. Hence, data privacy challenges can currently only be tackled on higher application layers or with dedicated hardware.

In this project, we aim to add advanced functionality to the network layer using NetFPGA.[2] You will get to play around with this cutting-edge research hardware and try to extend the functionality of current programmable network devices. After overcoming the technicality with NetFPGA, you will have a chance to implement your own ideas on the device that you built! At this step, you can offload a higher-level functionality to the data plane, or come up with your original protocols, algorithms, or system designs.

If you like FPGAs and you are motivated to implement your own ideas into network hardware, please contact us for further details!

Requirements

- a strong background in FPGA programming
- experience with P4 programming is advantageous (but not strictly required)
- thinking out of the box, independent problem solving

Contact

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References

[1] https://barefootnetworks.com/products/brief-tofino/
[2] https://netfpga.org/