Advantages of Reconfigurable Hardware

IP 9 deals with the design of Communicating Embedded System (CES) such as Terminodes. This work investigates reconfigurable hardware in wireless network nodes.

Project Goal

A Terminode is ...
• a heterogeneous device
• a terminal to user (audio- and video coding, sensor data processing, ...)
• a network node (store and forward, QoS routing, cryptography, ...)

Terminodes require ...
• occasionally a high amount of local processing power
• flexibility to reprogram and update

Performance / Flexibility Trade-Off

Goal: Design of Flexible Terminode Platform for High Performance Streaming Applications

Research Issues

Target Hardware Architecture

CPU + OS, IPAQ h3970:
• Intel xScale @ 100-400 MHz
• PocketPC 2003 (WinCE 4.1)
• real-time operating system
• integrated Bluetooth IF
• optional WLAN

Reconfigurable Hardware:
• Xilinx Spartan II FPGA
• CPLD, 1Mbit SRAM, 8Mbit Flash

Programming Model - Virtual Machine

Model of Computation:
• Focus on stream-based applications, specified as Process Networks.
• Task coordination language:
  - in interpretable format
  - clear semantics to check real-time properties

HW/SW Tasks:
• Task implementations are platform optimized:
  - no performance loss
• downloadable over wireless network

Abstraction Layer:
• Virtualization of reconfigurable logic
• provides a common interface to the virtual machine

Prototyping Platform

CPU + OS, IPAQ h3970:
• Intel xScale @ 100-400 MHz
• PocketPC 2003 (WinCE 4.1)
• real-time operating system
• integrated Bluetooth IF
• optional WLAN

Reconfigurable Hardware:
• Xilinx Spartan II FPGA
• CPLD, 1Mbit SRAM, 8Mbit Flash

Publications / Related Work

Publication:

Wireless Network Nodes and Virtual Machine:
• Levis, P.; Culler, D.: Mate: a tiny virtual machine for sensor networks, SIGPLAN Notices, Oct. 2002; difference to this work: focus on code size minimization, assembler-like code, not suited for high performance tasks.

Reconfigurable Computing:
• Yajun, H. et al.: A hardware virtual machine for networked reconfiguration, RSP’00, June 2000; difference to this work: direct byte code interpreter for FPGA circuits, virtualization of FPGA-routing, performance loss.
• Nollet, V. et al.: Designing an operating system for a heterogeneous reconfigurable SoC, IPDPS’03, April 2003; difference to this work: no specific model of computation.

IP9 Communicating Embedded Systems
Reconfigurable Hardware in Wireless Networks
Matthias Dyer
Computer Engineering and Networks Laboratory, ETH Zurich