Cluster 2

Interface-Based Rate Analysis of Embedded Systems

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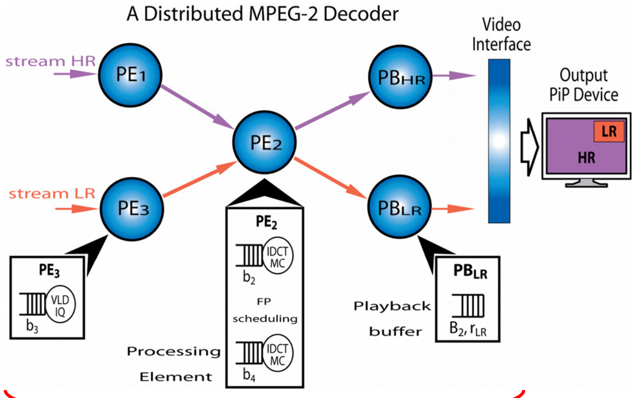
Introduction

Example Application Scenario

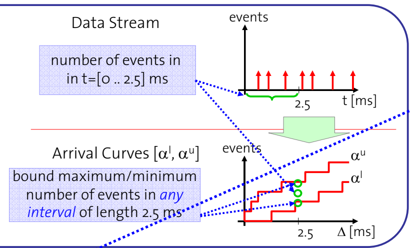


Problems

Analyse a **heterogeneous stream processing distributed embedded system** for:

- Minimum and sufficient buffer spaces in each node
- Maximum end-to-end delays
- Minimum and sufficient resource capabilities for each node
- Maximum stream data rates handled by the system

Method



1. Use **Variability Characterization Curves** to model: **Data streams** – characterize the burstiness in the arrival pattern of events; **Resource capabilities** – characterize the variability in the service provided by a hardware resource; **Buffer readouts** – characterize the variability of the number of items being read from a buffer

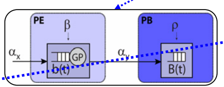
assumed values

$$\begin{cases} \alpha_x^{lA} = (\rho^{uG} - B_0) \oslash \beta^{lG} \\ \alpha_x^{uA} = \min\{\beta^{lG} \otimes (\rho^{lG} + B_{max} - B_0), \beta^{lG} + b_{max}\} \\ \beta^{lA} = \max\{(\rho^{uG} - B_0) \oslash \alpha_x^{lG}, \\ \qquad \alpha_x^{uG} \oslash (\rho^{lG} + B_{max} - B_0), \alpha_x^{uG} - b_{max}\} \\ \rho^{lA} = (\alpha_x^{uG} \oslash \beta^{lG}) - (B_{max} - B_0) \\ \rho^{uA} = (\alpha_x^{lG} \otimes \beta^{lG}) + B_0 \end{cases}$$

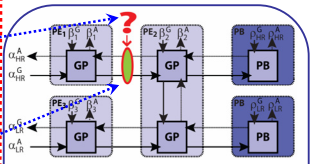
4. Define **Real-time Calculus** relations (based on Network Calculus) in the abstract components to allow for distributed systems and explicitly model the buffer sizes

2. Define reusable **abstract components** that model the real-time properties of concrete HW/SW components: **Processing elements** – components which contain one or more greedy processors; **Readout buffers** – components containing only a buffer

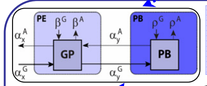
abstract component of one PE and one PB



check compatibility of Rate Interfaces (predicates =? true)

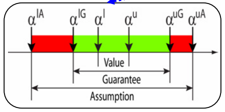


5. Compose a **model of the system from the components** and check compatibility at each interface connection while composing



assume/guarantee predicate: guaranteed values are enclosed by the assumed (rates compatible)

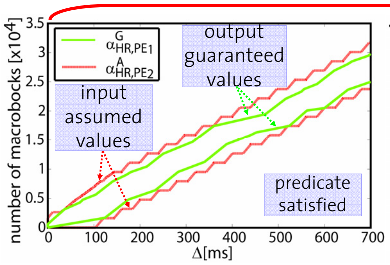
Rate Interfaces specified for a component of one PE and one PB

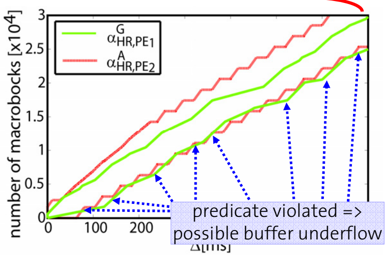


3. Define **Rate Interfaces** based on Real-Time Interfaces and Assume/Guarantee Interfaces (Henzinger et.al.) for the abstract components with **input and output predicates** which define compatibility of two components: **their interfaces are compatible if the rates of the outputs of one interface are compatible with the rates of the inputs of the other interface**. Compatibility guarantees buffer underflow and overflow constraints

Experimental Results

- **Check the interfaces between PE1 and PE2 given different initial buffer fill-levels in PBhr**
- 2 video streams (704x576 pixels) in a picture-in-picture MPEG-2 decoder with 3 processing elements and 2 readout buffers
- 704x576 pixels, CBR, 8Mbps, 25fps, SimpleScalar models with the PISA instruction set, macroblock granularity
- RTC Toolbox and Matlab – www.mpa.ethz.ch





References

- S. Chakraborty, Y. Liu, N. Stoimenov, L. Thiele, and E. Wandeler. Interface-based Rate Analysis of Embedded Systems The 27th IEEE Real-Time Systems Symposium (RTSS), Rio de Janeiro, 5-8 Dec 2006
- L. Thiele, E. Wandeler, and N. Stoimenov. Real-time Interfaces for Composing Real-time Systems The 6th ACM Conference on Embedded Software (EMSOFT), Seoul, 22-25 Oct 2006

FNSNF
Fonds national suisse
Schweizerischer Nationalfonds
Fondo nazionale svizzero
Swiss National Science Foundation
EPFL École Polytechnique Fédérale de Lausanne
Unil Université de Lausanne
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich
u^b Universität Bern
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