Predictable Wireless Embedded Platforms

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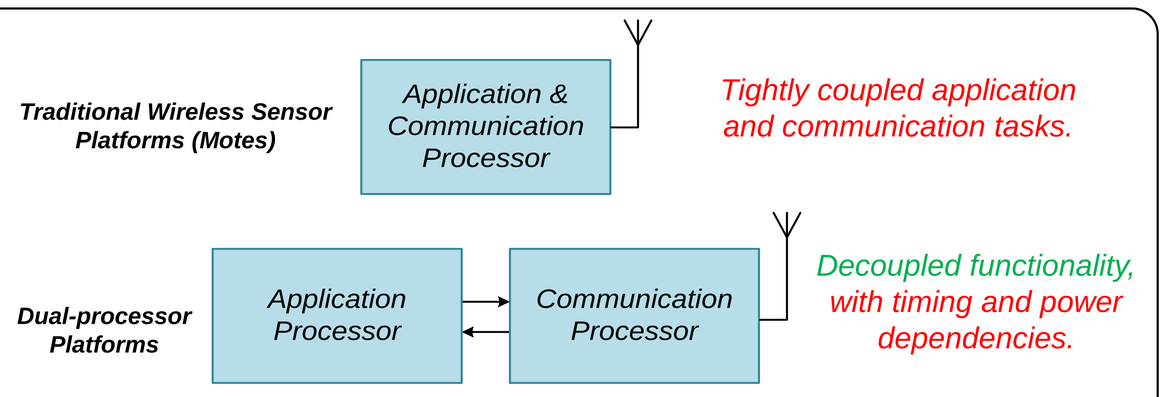
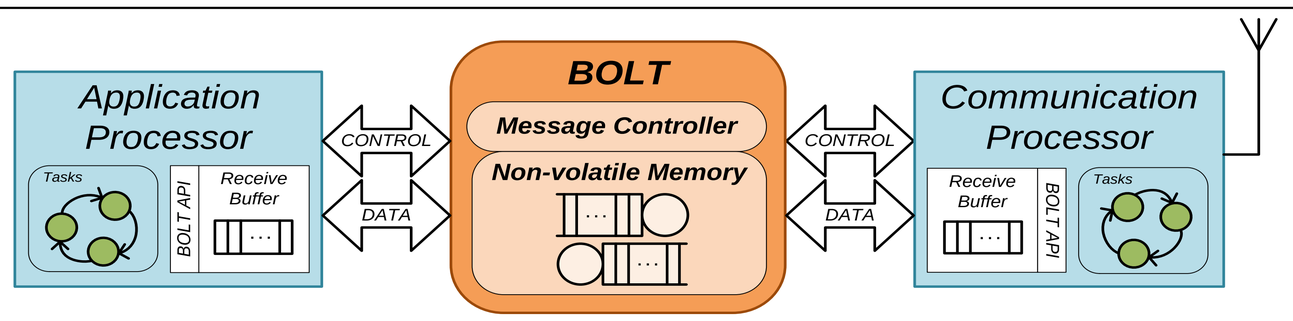
> Motivation

- *Traditional wireless sensor platforms enabled initial simple sense-and-send applications, e.g. environmental monitoring, on a single processor.*
- *In today's distributed embedded system landscape, the ever **increasing resource demand** and the requirements for **run-time adaptability** and **low power consumption** encourage the adoption of **multi-processor** architectures.*
- *However**, interference on shared resources**, e.g., interconnects and memory, seriously hampers modularity, predictability and energy-proportional system performance.*



> Interface Architecture



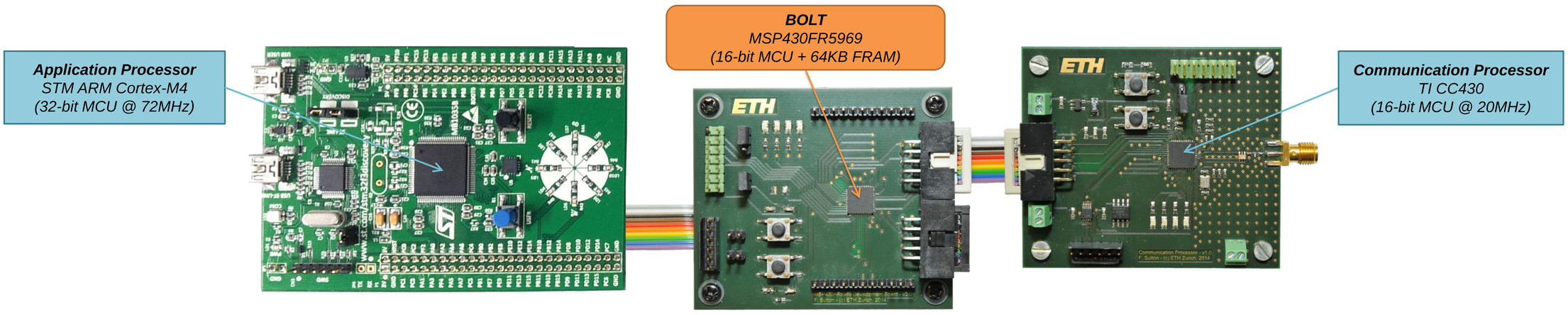
*Decoupled application and communication tasks with respect to **time, power and clock.***

***BOLT** is the first processor interconnect that allows any two arbitrary processors to execute within their **own time, power and clock domains**, while supporting **predictable inter-processor communication** through asynchronous message passing.*

- ✓ ***Avoidance of resource interference***
- ✓ ***Tight bounding of unavoidable interference***
- ✓ ***Formal specification of communication interface***

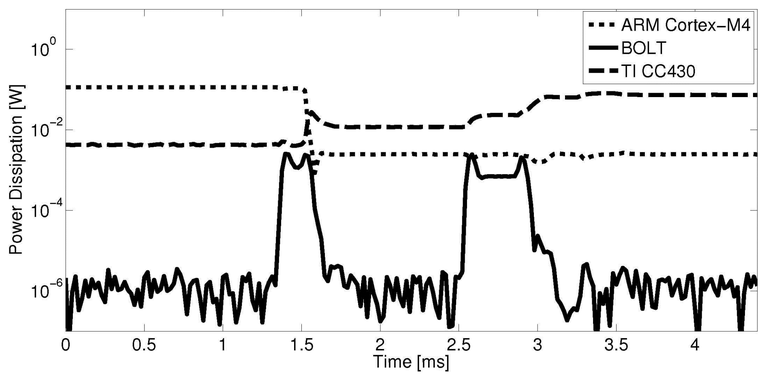
*Paradigm shift towards **compositional** construction and **predictable** operation of heterogeneous **ultra low-power** wireless sensor platforms.*

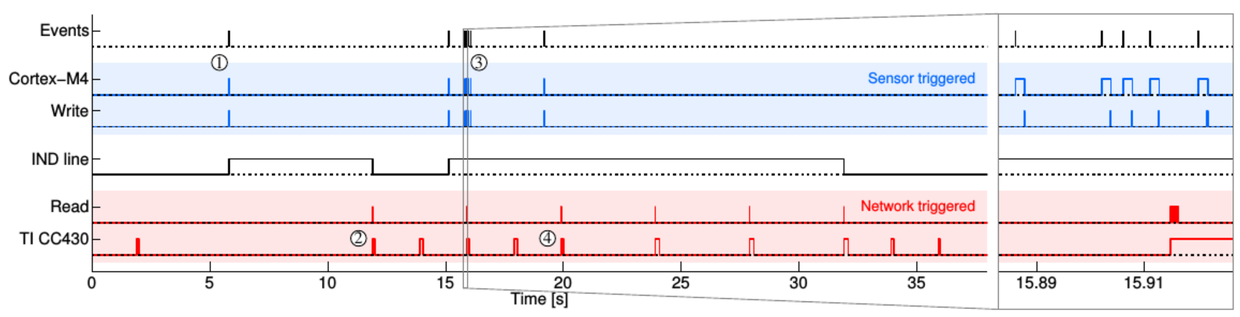
> Prototype Evaluation



Power Analysis:

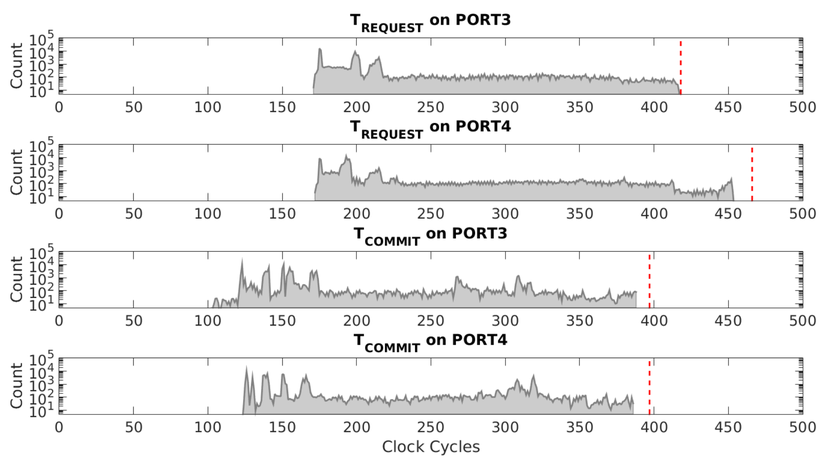
- *Ultra-low **1.2µW** @ **3.0V** power dissipation of BOLT in idle mode.*
- *Non excessive **1.1mW** @ **3.0V** power dissipation during message operations.*
- *Elaborate application and communication processor selections will lead to optimal energy efficiency while sustaining reactivity.*





Timing Analysis:

- *System modeling with timed automata.*
- *Formal verification of timing properties (Uppaal model checker).*
- *Worst case execution bounds tightly capture measured delays.*



BOLT in Action:

A wireless sensing application obliged to persist reactive to asynchronously incoming sensor events on the application processor side, network events on the communication processor side and committed to optimal energy efficiency.

(1) Single sensor event → communication processor in sleep-mode until next scheduled transmission round (2).

(3) Sporadic sensor event burst, concurrent network event → simultaneous processor activities and BOLT communication.

(4) Network load balancing → sink informs communication processor to reduce periodicity.