

Semester/Master Thesis

A Fast Temperature-guaranteed Mapping Framework for Many-core Systems

Overview

Devising a fast design space exploration framework that guarantees the worst-case temperature.

Motivation

As the power density of circuits has been continuously increasing leading to high on-chip temperature, it is crucial to consider the temperature issue in many-core system design. In our lab, we developed a multi-core thermal analysis technique based on modular performance analysis (MPA) framework. Once the workload specification and task-processor mapping is given, we can calculate the worst-case temperature of the system. As there are too many candidate mappings to be evaluated in design space exploration (DSE) phase, it takes unacceptably long time to naively evaluate worst-case temperatures of all candidates.



In this work, we propose to develop a fast yet temperature-guaranteed DSE method based on the legacy framework, DOL/DAL (<http://www.tik.ee.ethz.ch/~shapes/dol.html>). The idea is to exclude the time-consuming thermal evaluation part out of the main DSE loop. That is, the new proposed DSE now consists of two decoupled part. The first part is to find out the workload bounds for all cores that are safe in terms of worst-case temperature. The basic thermal analysis technique can be reused here without any modification. The main challenge is how to adjust the workloads when they do not meet the temperature constraint. Once the safe workloads are found, then we just use these as *constraints* in main DSE.

Project Description

Your tasks can be summarized as follows:

1. Devising a systematic method to adjust workload specification to reduce the worst-case temperature.
2. Automation/evaluation of the 2-phase DSE technique and evaluation of the proposed approach.

Requirements

You should be familiar with C and the Java programming language. The basic knowledge on MPA would be of help (taught in Hardware-Software Co-Design lecture).

Contact

Interested? Please do not hesitate to contact us!

Advisors: Hoeseok Yang, ETZ G 86, hoeseok.yang@tik.ee.ethz.ch

Professor: Prof. Dr. Lothar Thiele, ETZ G 87, thiele@tik.ee.ethz.ch