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Distributed Application Layer: Adaptive Mapping of Multiple Streaming Applications onto On-Chip Many-Core Systems

How to program and design such a system so that it is analyzable and efficient?

Workload Specification
- Execution scenarios to deal with multiple applications
- Each application is specified as a Kahn process network

Architecture Specification
- Hierarchically organized
- Non-uniform memory access (NUMA) design
- Examples: Intel SCC / Xeon Phi
- STThorn (P2012)
- NVIDIA Fermi architecture

Run-Time
- Hierarchically organized run-time manager:
  - One controller per communication layer
  - Each controller has an individual database with its relevant mapping information
  - Events processed by the first controller that can handle the event
- Fault management:
  - Mapping towards virtual architecture
  - Redundant tiles to remap the processes

Hierarchical Decomposition
- How does hierarchical decomposition affect the performance of the mapping strategy?
- Performance of holistic mapping optimization relative to hierarchical mapping optimization:

Evaluation
- Fully automated tool chain targeting Intel’s SCC processor

Deployment
- Hierarchical Decomposition
- Different Levels of Parallelism
  - Motion-JPEG (MJPEG) decoder application
  - How does the degree of parallelism affect the throughput?

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