Computer Engineering Group at ETHZ

Personnel

- Prof. Dr. Lothar Thiele
- Monica Fricker
- Dr. Iuliana Bacivarov
- Dr. Jan Beutel
- Dr. Kai Lampka
- Dr. Beat Pfister
- Dr. Jian-Jia Chen (from 2008)
- Thomas Ewender
- Michael Gerber
- Min Guo
- Wolfgang Haid
- Sarah Hoffmann
- Kai Huang
- Tobias Kaufmann
- Roman Lim
- Andreas F. Meier
- Clemens Moser
- Simon Perathoner
- Harald Romsdorfer
- Andreas Schranzhofer
- Nikolay Stoimenov
- Matthias Woehrle
- Mustafa Yuecel

Summary

The Computer Engineering Research Group (TEC) concentrates on design, engineering methodologies and tools for embedded systems. TEC is active in embedded software for distributed real-time systems as well as in the design of mobile information and communication systems.

In particular, we are interested in analytic methods for performance evaluation, multiprocessor system-on-chip and sensor networks. In addition, the research group is investigating applications which benefit from multi-objective optimization such as the design of embedded system architectures and embedded software under conflicting criteria. Finally, TEC is engaged in the area of speech processing, i.e. text-to-speech
synthesis and speech recognition.

The research of TEC is funded by direct industry projects, various EU projects, KTI (Swiss Confederation's Innovation Promotion Agency), SNF (Swiss National Science Foundation) and NCCR (Swiss National Research Center).

Research Areas

Sensor Networks

The computer engineering research group investigate an extreme area in the design space of communicating objects: low energy, small size, and large population. In particular, we approach research problems in the design, implementation and deployment of wireless ad-hoc networks. Major directions in our research are

- Development of the BTnode platform, an autonomous wireless communication and computing platform based on a Bluetooth radio, a low-power radio operating in ISM band and a microcontroller.
- Methods and tools to support the deployment and programming of large-scale sensor networks. Its goal is to replace the current "trial-and-error deployment practice" with a systematic approach.
- Theoretical investigations related to time synchronization in large-scale distributed networks.
- Scheduling theory for energy harvesting systems.
- Methods to design dependable sensor networks, e.g. for safety applications. Here, we investigate novel protocols on all layers that are adaptive, give performance and delay guarantees and are adaptive to changes in the environment.
- The Sensor Network Platform Kit aims at creating a wireless sensor network out-of-a-box for basic low power sensing and data collection applications, e.g. environmental monitoring.
- Today, we are investigating three applications projects: “Permasense” is a typical environmental monitoring application in an extreme outdoor environment where a wireless sensor network is used to investigate permafrost in the Swiss Alps. “Smart Buildings” is an indoor monitoring application to investigate the heat, ventilation, cooling processes in buildings. Furthermore, the project takes an active role in the international TinyOS based wireless sensor network community. “Safety Networks” is a joint project with Siemens Building Technologies aiming at a sensor network for fire detection with high expectations in terms of safety, real-time operation, scalability and low energy operation.

Performance Analysis

In the design of embedded systems, we are faced with major changes: Embedded systems are getting increasingly distributed and networked and they are comprised of many cooperating individual components. Examples of these systems are networks of sensors and actuators, building automation, car communication networks, personal health care, environmental monitoring, ubiquitous and pervasive computing. There are several fundamental problems that make the design of distributed embedded systems difficult:

- handling non-functional and resource constraints,
- design under multiple conflicting criteria,
- trade-off between average performance and predictability.

It appears that conventional computer science and engineering methods are at their limits. The scaling up in distributivity and size asks for a paradigm shift in models and methods. One of the major challenges in the
The design process of embedded systems is to estimate essential characteristics of the final implementation early in the design. Typical questions faced by a designer during a system-level design process are: Which functions should be implemented in hardware and which in software (partitioning)? Which hardware components should be chosen (allocation)? How should the different functions be mapped onto the chosen hardware (binding)? Do the system-level properties meet the non-functional requirements? As distributed systems are heterogeneous in terms of the underlying execution platform, the diverse applications running concurrently, the different scheduling and arbitration policies used, modularity is a key requirement for any performance analysis method. We are investigating analytic methods based on network calculus and real-time calculus that allow worst case and best case analysis results of distributed embedded systems.

**Multiprocessor Systems**

In order to handle the ever increasing complexity of applications found in modern embedded systems, the focus is moving away from single processor implementations towards heterogeneous multiprocessor system-on-chip (MPSoC) architectures. While offering high scale integration, high computing power and low power consumption, designers also face new challenges. In particular, a mapping phase is required which cannot be found in single processor design but is essential to exploit the performance potentials of MPSoC architectures. We are developing a framework, termed distributed operation layer (DOL), which seamlessly integrates the mapping of real-time applications onto MPSoC architectures into a complete design flow. The focus is on the mapping optimization that together with appropriate performance evaluation strategies allows to compute mappings with a guaranteed performance. Besides the mapping optimization, our framework provides models for application programmers, enabling them to write parallel applications that efficiently execute on parallel architectures.

**Speech Processing**

The mission of the speech processing group is to advance text-to-speech synthesis, speech recognition, and speaker verification, both in research and in technology development. The relation between speech and text is in the focus of our work. We pursue mainly interdisciplinary approaches that require competence in fields as diverse as digital signal processing, statistical modeling and computational linguistics (e.g. grammar formalisms and parsers for natural languages). The extensive application of rule-based linguistic knowledge in morphology and syntax is precisely what distinguishes our work from the work of most other speech research groups. Several ongoing projects (e.g. polySVOX, RULAMO and SpVeri) contribute to our long-term aims.

**Major Hardware and Software Products**

- PISA: A Platform and Programming Language Independent Interface for Search Algorithms
- BTnodes - A Distributed Environment for Prototyping Ad Hoc Networks
- MPA: Modular Performance Analysis with Real-Time Calculus
  [http://www.mpa.ethz.ch/](http://www.mpa.ethz.ch/)

**Successful Startups**

- A4M applied formal methods: [http://www.a4m.biz](http://www.a4m.biz)
- CIP System AG: [http://www.ciptool.ch](http://www.ciptool.ch)
- SVOX AG: [http://www.svox.com](http://www.svox.com)

**Teaching Activities**
Computer Engineering I (Bachelor D-ITET)
- Embedded Systems (Bachelor D-ITET/D-MAVT)
- Hardware-Software Codesign (Master D-ITET/D-INFK)
- Speech Processing I (Master D-ITET/D-INFK)
- Speech Processing II (Master D-ITET/D-INFK)
- Studies on Mechatronics (Bachelor D-MAVT)
- PPS Mindstorms (Bachelor D-ITET)
- PPS Speech Recognition (Bachelor D-ITET)
- Mobile Information and Communication Systems (PhD Level D-INF/D-ITET)

External Funding
- Safety Critical Sensor Networks for Building Applications
  Start Date: 1.6.2006. Duration: 36 months. Partners: Siemens CH, Siemens BT, CSEM
- Analytic Performance Estimation of Embedded Computer Systems
  Start Date: 1.4.2004 / renewed 1.10.2007. Duration: 36 months
- NCCR Mobile Information and Communication (MICS), including the Sensor Network Platform Kit (SNPK) project
  Long Term Research Program until 2009 with prolongation
- EU Network of Excellence in Embedded System Design ARTIST2 / ARTISTDesign
  Long Term Research Program until 2012
- EU Project SHAPES: A scalable HW/SW design style for future Embedded Systems
  Start Date: 1.1.2006. Duration: 42 months. Universities, ATMELE, ST Microelectronics, Thales, Target Compilers, FhG, MedCom, Pie Medical
- EU Project PREDATOR: Design for Predictability and Efficiency
  Start Date: 1.1.2008. Duration: 36 months. Partners: Universities, EADS/Airbus, Bosch, ABSINT
- EU Project COMBEST: COMponent-Based Embedded Systems design Techniques
- Baseband Computation Platform for Software Defined Radio
- VoiceTools: Methods and Tools for Improved Concatenative Text-to-Speech Synthesis
  Start Date: 1.10.07. Duration: 36 months
- PROSO: Prosody Control for Polyglot Speech Synthesis
  Start Date: 1.10.07. Duration: 36 months
- RULAMO: Rule-Based Language Model for Speech Recognition
  Start Date: 1.4.06. Duration: 30 months
- NCCR IM2.AP: Speaker Verification
  Start Date: 1.1.06. Duration: 24 months
- Approximated total third party funding per year: 2 MCHF

Completed PhDs


Short CV Lothar Thiele

Present Position

- Head of Computer Engineering and Networks Lab

Degrees/Higher Education

- 1987 Habilitation (venia legendi) for network theory with a thesis entitled «Algorithmically specialized VLSI structures».
- 1984 Dr.-Ing. from Technical University Munich with a thesis entitled «Analytische Netzwerksynthese». Supervisor: Prof. R. Saal.
- 1981 Dipl.-Ing. in Electrical Engineering, Technical University Munich, Germany.

Professional Career

- 1994–present Professor at ETH Zurich in the area of computer engineering.
- 1987 Research Associate, Stanford University. Member of the Information Systems Lab. in the research group of Prof. Tom Kailath. Research in the area of information technology.
- 1981–1986 Research Assistant in the area of network theory and circuit design, Technical University Munich.

Professional Activities

- Chair of ACM SIGBED (Special Interest Group Embedded Systems)
- Organization of various workshops and conferences (general chair, program chair, member of PC)
- Leading and co-leading of various large-scale research programs, such as Sonderforschungsbereich SFB 124 «VLSI and Parallelism» in Saarbrücken, NCCR MICS (Mobile Information and Communication Systems).
- Steering Committee of the International Master in Embedded Systems ALARI, Lugano, Switzerland.
- Member of the Advisory Board of the Embedded Systems Institute, Eindhoven, The Netherlands.
- Leading evaluation committees of various faculties in Information Technology and Electrical Engineering (Kaiserslautern, Darmstadt, Karlsruhe).
Major Honors and Awards

- 2005 Honorary Blaise Pascal Chair of the University Leiden, The Netherlands
- 2004 Member of the German Academy of Natural Sciences, Leopoldina
- 2000/1 IBM Faculty Achievement Award
- 1988 Browder J. Thompson Memorial Prize Award of the IEEE
- 1987 Outstanding Young Author Award of the IEEE
- 1986 Award of the Technical University Munich for the best PhD thesis
- 1977 Studienstiftung des Deutschen Volkes

Publications (overview)

- 60 Refereed Journal Publications
- 143 Refereed Conference Publications
- 277 Publications in total
- 1249 citations (CiteSeer), 764 citations (ISI Web of Knowledge), h-index 34 (PoP)

Research areas

- Embedded Systems and Embedded Software
- Bio-inspired Optimization Techniques
- Multi-objective Optimization
- Mobile Computing and Sensor Networks

Committees (ETHZ)

- Delegate of the President of ETH Zurich for the appointment of professors
- Member of University Senate (Hochschulversammlung)
- Member of the Research Commission (Forschungskommission)
- Member of the Planning Commission (Planungskommission).
- Member and Head of Study Committee of Dept. ITET (until 2001)
- Study Director of D-ITET (2001–2006)
- Representing ETH Zurich in affairs related to Bologna treaty
- Representing D-ITET in IDEA-League, an educational network of the four leading universities in Europe.
- Member of Konferenz des Lehrkörpers, Vice President (until 2006)
- Initiating and leading the PhD School in C3 (Computer, Control and Communications) of D-ITET

Personnel (research group)

- Completed PhD (2005–2006) 10
- PhD students (current) 11
- PostDocs (current) 4

Main Publications (2004-2007)

Journal


- Karl Aberer, Gustavo Alonso, Guillermo Barrenetxea, Jan Beutel, Jacques Bovay, Henri Dubois-


Conference


Lothar Thiele, Iuliana Bacivarov, Wolfgang Haid, Kai Huang: Mapping Applications to Tiled


Iuliana Bacivarov, Michael Beckinger, Wolfgang Haid, Kai Huang, Lothar Thiele: Distributed Operation Layer: Optimal Mapping of Parallel Applications onto Heterogeneous Multiprocessor Tile-Based Architectures. DATE07 Workshop, Nice, France, April, 2007.


Ernesto Wandeler, Lothar Thiele: Abstracting Functionality for Modular Performance Analysis of


Alexandre Maxiaguine, Simon Künzli, Lothar Thiele: Workload Characterization Model for Tasks with Variable Execution Demand. Design Automation and Test in Europe (DATE), IEEE Computer


