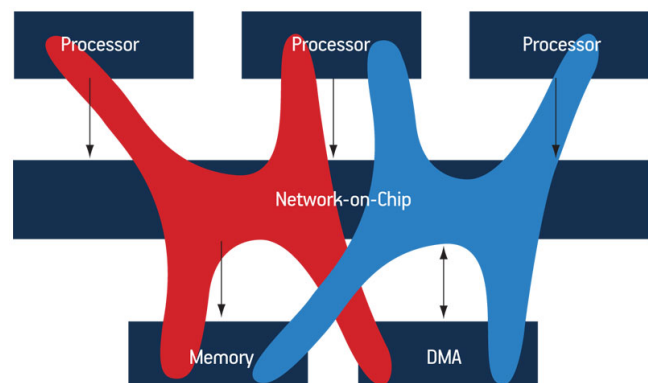


Semester/Master Thesis:

Platform benchmarking for real-time applications

The Problem: Commercial computing platforms become increasingly multi-core, featuring up to tens or hundreds of processing cores, see e.g., the Kalray MPPA-256, the Tiler TILE64, or the Adapteva Epiphany chip. Typically such platforms are optimized for average performance in terms of hardware and runtime environment. However, when deployed for real-time safety-critical applications, the worst-case timing behavior on them has to be analysed and bounded. This task is far from trivial, since the applications that run concurrently across the cores interfere with each other in complex ways through the shared platform resources, e.g., when competing for access to a shared memory or a link of a network-on-chip, or when invalidating each other's cache lines in a shared L2-cache. For ensuring that the applications meet their real-time requirements, accurate models of all platform resources are needed. Such models, though, are almost never provided by the vendors.

The Thesis: The goal of this thesis is to develop low-level benchmarks for commercial-off-the-shelf platforms, for which available documentation is limited. The benchmarks should be designed so as to maximally stress the shared resources, hence revealing their worst-case timing behavior. One such benchmark could trigger maximal traffic in a network-on-chip or the maximum number of parallel accesses to a shared DRAM bank. The desired outcome is an accurate model (arbitration policy, access time, ...) of each shared resource that can be used for worst-case timing analysis of the applications that run on the platform.



Requirements:

- Interest in "reverse-engineering" of hardware resources.
- Low-level C/C++ programming skills.
- Data analysis, e.g., Matlab or Mathematica.

Interested? Please have a look at <http://www.tec.ethz.ch/research.html> and contact us for more details!

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