

Master Thesis:

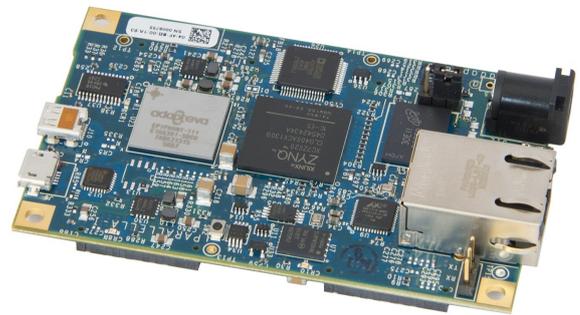
Hardware/software co-programming on the Parallella platform

Implement an ultrasound imaging algorithm for the “multi-core Raspberry Pi”, using all available computation resources like CPU, accelerator chip and FPGA.

The Parallella is a new and modern low-power platform similar to the Raspberry Pi. It features a dual-core ARM A9 processor running Linux, a powerful FPGA and a 16-core accelerator chip called “Epiphany III”. All these components cores are linked tightly to each other, allowing fast and reliable communication.

On this platform, we would like to implement medical ultrasound imaging, i.e. the reconstruction of images out of ultrasound echo signals. The groups of Lothar Thiele and of Luca Benini have looked into this from the software and the hardware angle, respectively. The Parallella platform now offers the possibility to combine these efforts to a joint hardware/software approach.

Task: This thesis, which is offered collaboratively by both groups, will be about finding the right balance between (reconfigurable) hardware and software implementation for a given ultrasound imaging algorithm, considering the advantages and drawbacks of both. Existing code (VHDL description for hardware and C-based implementation for software) can be reused, but will have to be adapted. A concrete goal would be to have a running version of the algorithm on the Parallella board, optimally using all components of the latter. All this would involve the following steps:



1. Get familiar with the Parallella platform and understand its architecture.
2. Port the software implementation of the ultrasound algorithm to the Parallella.
3. Gradually replace individual parts of the application by accelerator circuits on the FPGA.
4. Optimise the balance of software and hardware (particularly the work distribution between ARM, Epiphany and FPGA), looking at different goals like data throughput or power consumption.
5. Draw conclusions comparing hardware and software implementations and find the optimal field of application for each of both.

If desired, extensions to the work, e.g. linking two Parallellas for better performance, are possible.

Requirements: You should be familiar with VHDL (e.g. from the VLSI lecture) and with C/C++. Knowledge about FPGA or low-level programming (e.g. from microcontrollers) would be an asset.

Interested? Please have a look at www.tec.ethz.ch/research.html or at www.iis-projects.ee.ethz.ch/index.php/Category:Digital and contact us for more details!

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Further Reading

- Parallella platform: <http://www.parallella.com/>