

Semester / Master Thesis:

Advanced State Retention for Transient Systems

The last years have seen an increasing demand for batteryless devices that reliably execute complex applications. This is the upcoming field of transient computing systems. In our group, we have developed an energy management unit (EMU) [1] which accumulates minimal amounts of energy (harvested e.g. from small solar panels) and then powers a small electronic device for long enough to execute atomic tasks like taking pictures or sending radio packets. As we explore multi-core transient computing systems to execute even more complex applications, one of the key challenges that remains unsolved is how to efficiently execute non-atomic tasks, i.e. tasks that can be “paused” depending to harvesting conditions. This involves keeping track of a complex program state which is spread out over multiple memory banks. Conventional strategies, which copy the entire program state to a non-volatile memory only when power is about to run out, are no longer viable due to the huge overhead of backing up multiple memory banks.

Your Project: During this project, which is a collaboration between TIK and IIS, you will learn about state retention, multi-core programming frameworks, and energy harvesting. Your task will be to develop novel algorithms to keep track of an application’s state and parallelize processing with novel check-pointing techniques. The goal is to implement non-atomic task execution in given image processing application and to compare the new version to the existing, atomic version.

Requirements: You should be highly motivated, have experience with embedded system programming in C, and be comfortable working with lab equipment such as oscilloscopes.

Interested? Please have a look at <http://www.tec.ethz.ch/research.html> and contact us for more details!

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References

- [1] [Dynamic Energy Burst Scaling for Transiently Powered Systems](#). Gomez, A. et al. Proc. DATE 2016.
- [2] [QUICKRECALL: A Low Overhead HW/SW Approach for Enabling Computations across Power Cycles in Transiently Powered Computers](#). Jayakumar H. et al. Proc. VLSID 2014.

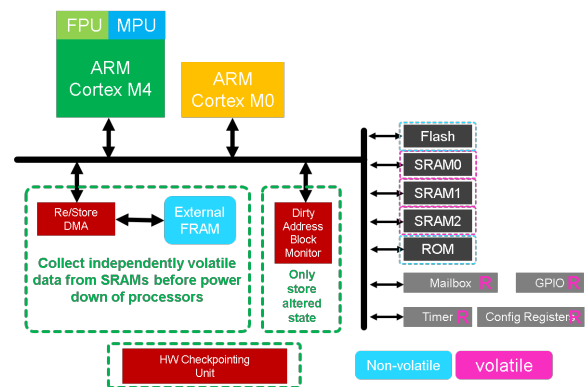


Figure 1: Multi-Core platform with multiple volatile memory domains.